ISED2011 Accepted Papers

Varanasi Suresh Kumar and Satyam Mandavilli. Process Variation Tolerant SRAM cell design
Indrajit Pan, Parthasarathi Dasgupta, Hafizur Rahaman and Tuhina Samanta. Ant Colony Optimization Based Droplet Routing Technique in Digital Microfluidic Biochip
Ramkumar Jayaraman, Handi Kartadihardja and Douglas L. Maskell. Performance-power design space exploration in a hybrid computing platform suitable for mobile applications
Hafizur Rahaman and Debaprasad Das. Crosstalk and Gate Oxide Reliability Analysis in Graphene Nanoribbon Interconnects
Ramracksha Tripathi, Shivshankar Mishra and S. G. Prakash. A Novel 14-Transistor Low-Power High-Speed PPM Adder
Bimal Kumar Meher and Pramod Kumar Meher. A NEW LOOK-UP TABLE APPROACH FOR HIGH-SPEED FINITE FIELD MULTIPLICATION
Saraju Mohanty and Elias Kougianos. PVT-Tolerant 7-Transistor SRAM Optimization via Polynomial Regression
Pable S.D and Mohd. Hasan. Performance analysis of ultralow-power mixed CNT interconnects for scaled technology
Wei Jhih Wang and Chang Hong Lin. An Improved BitMask Based Code Compression Algorithm for Embedded Systems
Zubair Akhter and Nagendra Pathak. Concurrent Dual-Band Transmitter for 2.4/5.2 GHz Wireless LAN Applications
Jyotsna Kumar Mandal and Somnath Mukhopadhyay. A Novel Variable Mask Median Filter for Removal of Random Valued Impulses in Digital Images(VMM)
S. Srinivasan, V. Kamakoti and A. Bhattacharya. Towards Improved Solutions for Generalized Placement Problem
K.P Karthik, Rangababu P. and Samrat Sabat. System on Chip implementation of Adaptive moving average based multiple-model Kalman filter for denoising Fiber Optic Gyroscope signal
Aminul Islam and Mohd. Hasan. Low Active Power High-Speed Cache Design
Uttam Mondal and Jyotsna Kumar Mandal. A Message embedded Authentication of Songs to Verify Intellectual Property Right(MEAS)
Jyotsna Kumar Mandal and Subhankar Ghatak. A Novel Technique for Secret Communication through Optimal Shares using Visual Cryptography (SCOSVC)
Manish Patil, Shaila Subbaraman and Shirish Joshi. Exploring Integrated Circuit Verification Methodology for Verification and Validation of PLC Systems
Ashok Kumar Suhag and Vivek Shrivastava. Delay Testable Enhanced Scan Flip-Flop: DFT for High Fault Coverage
Harish Yagain and Srinivas Donapati. Addressing the Interoperability Issues While Using JPEG-XR
Nachiketa Das, Pranab Roy and Hafizur Rahaman. Runtime Congestion and Crosstalk Aware Router for FPGA Using Jbits3.0 for Partial Reconfigurable Application

L Unnikrishnan. The Design of an Efficient Parallel Resonant DC/DC Boost Converter for High Frequency Application
Amrita Som and Amlan Chakrabarti. A New BSQDD Approach for Synthesis of Quantum Circuit
Surajit Kumar Roy, Chandan Giri, Arnab Chakraborty, Subhro Mukherjee and Hafizur Rahaman. Optimizing Test Architecture for TSV based 3D Stacked ICs using Hard SOCs
Surajit Kumar Roy, Chandan Giri, Sourav Ghosh and Hafizur Rahaman. Optimization of Test Wrapper for TSV based 3D SOCs
Chetan Vudadha, Sai Phaneendra Parlapalli, Syed E, Sreehari V, Moorthy Muthukrishnan N and Srinivas Mb. A Reconfigurable INC/DEC/2's complement/Priority encoder Circuit with Improved Decision Block
Mamatha Samson. Adiabatic 5T SRAM
Anand Darji, A.N. Chandorkar and Shabbir Merchant. A High Speed and Lowpower 2-D DWT Architecture Optimised for 5/3 Filter Using Lifting Scheme
Mohammad Maghsoudloo, Hamid Reza Zarandi and Navid Khoshavi. Low-Cost Software-Implemented Error Detection Technique
Madhumita Sengupta and Jyotsna Kumar Mandal. Image Authentication using Hough Transform generated Self Signature in DCT based Frequency Domain (IAHTSSDCT)
Nayan Mujaidya. Instruction Scheduling on Variable Latency Functional Units of VLIW Processors
Jyotsna Kumar Mandal and Amrita Khamrui. A Data- Hiding Scheme for Digital Image using Pixel Value Differencing (DHPVD)
Parthajit Roy and Jyotsna Kumar Mandal. A Novel Fuzzy-GIS Model based on Delaunay Triangulation to Forecast Facility Locations(FGISFFL)
Shravan Kumar Karthik, Samrat Sabat and Siba K. Udgata. Performance study of Harmony Search algorithm for analog circuit sizing
Tarunkumar Lad, Anand Darji, Arun Chandorkar and S. Merchant. VLSI Implementation of Wavelet based Robust Image Watermarking Chip.
Sandeep Goud Surya, Sudip Nag, Sahir Gandhi, Dilip Agarwal, Gaurav Chatterjee and Ramgopal Rao Valipe. HIGHLY SENSITIVE ΔR/R MEASUREMENT SYSTEM FOR NANO-ELECTRO-MECHANICAL CANTILEVER BASED BIO-SENSORS
K.S. Reddy, M.S. Bharath, Subhendu Kumar Sahoo, Shantanu Sinha and Jaipol Reddy. Design of Low Power, High Performance FIR Filter using Modified Differential Evolution Algorithm
Szu-Ling Liu, Tsu Chang, Ying-Jen Chen and Albert Chin. High Performance RF Power Amplifier Using High Breakdown Voltage Asymmetric-LDD MOSFETs
Rajkumar Pant, Narayanan Komerath and Aravinda Kar. Application of Lighter-Than-Air Platforms for Power Beaming, Generation and Communications
Chitti Babu B and Samantaray S R. Design and Impementation of Low Power Smart PV Energy System for Portable Applications Using Synchronous Buck Converter
Himesh Joshi and Maryam Shojaei Baghini. Versatile Battery Chargers for New Age Batteries
Jayashree V and Dr Shaila Subbaraman. DCSFPSS Assisted Morphological Approach for Grey Fabric Defect detection and Defect Area Measurement for Fabric Grading
Mahesh Kumar Adimulam and Srinivas M.B. A Multiple-Bandwidth 10-bit SAR Analog to Digital Converter

Hemangee Kapoor and Sajeesh K. An Authenticated Encryption based Security Framework for NoC Architectures
Alok Baluni, Farhad Merchant, S.K Nandy and S Balakrishnan. A Fully Pipelined Modular Multiple Precision Floating Point Multiplier With Vector Support
Luo Sun, Jimson Mathew and Saraju Mohanty. An Intelligent Statistical Blockade Method for Fast Robustness Estimation and Compensation of Nano-CMOS Arithmetic Circuits
Rakesh V., Smitha K.G. and Vinod A.P.. Low Complexity Flexible Hardware Efficient Decimation Selector
Yalcin Yilmaz and Pinaki Mazumder. Threshold Read Method for Multi-bit Memristive Crossbar Memory
Dipak Kole, Hafizur Rahaman, Debesh K Das and Bhargab B. Bhattacharya. Derivation of Automatic Test Set for Detection of Missing Gate Faults in Reversible Circuits
Oleg Garitselov, Saraju Mohanty and Elias Kougianos. Bee Colony Inspired Metamodeling Based Fast Optimization of a Nano-CMOS PLL
Toshanlal Meenpal and Anup K Bhattacharjee. High Capacity Reversible Data Hiding using IWT
Manish Baphna. A Method to Reuse RTL Verification tests to validate Cycle Accurate Model
Pranab Roy, Rupam Bhattacharya, Hafizur Rahaman and Parthasarathi Dasgupta. A Best Path Selection Based Parallel Router For DMFBs
Manisha Pattnaik, Shashank Parashar, Vikas Mahor, Inder Chaudhry and Akanksha Chouhan. A Novel Low Power Noise Tolerant High Performance Dynamic Feed Through Logic Design Technique
Bibhash Sen, Mousumi Saha, Divyam Saran and Biplab K Sikdar. Synthesis Of Reversible Universal Logic Around QCA With Online Testability
Priyankar Ghosh, Aritra Hazra, Niraj Bhilegaonkar, Pallab Dasgupta and Chittaranjan Mandal. POWER-SIM : An SOC Simulator for Estimating Power Profiles of Mobile Workloads
Rosario Dhinesh George, Rosario Jagadeesh George and Srikanthan Thambipillai. A Low-Complexity Speaker-and-Word Recognition Application for Resource-Constrained Devices
Prabir Saha, Arindam Banerjee, Partha Bhattacharyya and Anup Dandapat. Vedic Divider: Novel Architecture (ASIC) for High Speed VLSI Applications
Pratibha Sawhney, Anup Bhattacharjee and Ganesh. Automatic Construction of Runtime Monitors for FPGA based Designs
Naveen Sudhish, Raghavendra Br and Harish Yagain. An efficient method for using Transaction level assertions in a class based verification enviorement
Manoj Meena, Dipankar - and Rohit Khanna. Nonlinear Inductance Measurement Using an Energy Storage Approach
Rohit Khanna, Dipankar - and Manoj Meena. Design of 0-1KV Controlled Voltage Source
Mohammad Hosseinabady, Jimson Mathew, Saraju Mohanty and Dhiraj Pradhan. Single-Event Transient Analysis in High Speed Circuits
Narayanan Komerath, Aravinda Kar and Rajkumar Pant. Antenna Considerations for Retail Beamed Power Delivery in India
Vishram Mishra, Lau Chiew Tong and Syin Chan. MAC protocol for Two level QoS support in Cognitive Radio Network
Satyajeet Nimgaonkar, Srujan Kotikela and Mahadevan Gomathisankaran. Energy Efficient Memory Authentication Mechanism in Embedded Systems

Hirak Patangia and Sri Nikhil Gupta Gourisetti. A Harmonically Superior Switching Modulator with Wide Baseband and Real-Time Tunability